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Code No: A5707

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, March/April-2011
ANALOG IC DESIGN
(VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks
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1.a) Explain the large signal modeling of a BJT and also the time required to remove the saturation region.
b) Derive the overall DC gain of a common gate amplifier. [12]

2.a) Explain about Wilson's current mirror model.
b) Explain the dominant frequency effects in Integrated Circuit. [12]

3.a) Explain about the telescopic cascode and folded cascode amplifier.
b) What are clock feed through errors? Explain the method of minimizing errors due to charge errors. [12]

4.a) Explain the operation of class AB fully differential OPAMP with neat circuit diagram.
b) Derive the -3dB frequency of a current feedback OPAMP. [12]

5.a) Explain about a BiCMOS Sample and Hold Circuit with a neat circuit diagram.
b) Consider the Sample and Hold Circuit of an open loop track and Hold realized using MOS technology. The input voltage V_{in} is a 20 MHz band limited signal with a 2v peak-peak amplitude. Assume that ϕ_{clk} is 100 MHz square wave with peak amplitude of ±2.5v with linear rise and fall times of 1.5ns. What is the maximum uncertainty of Sampling? Make the necessary Assumptions. [12]

6.a) Explain a two step A/D Converter with digital error capability.
b) Explain the Resistor-Capacitor Hybrid A/D Converter. [12]

7.a) Draw the block diagram of a Multistage Noise Shaping(MASH) architecture that realizes the third order noise shaping using a second order modulator and a first order modulator.
b) Briefly explain the linearity of two level converters with appropriate examples. [12]

8. Write short notes on any **TWO**
a) Common mode Feedback Circuits
b) Biquad Filters
c) Flash type A/D Converters. [12]

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